

WHAT IS CLAIMED IS:

1                   1.       A video encoder/decoder coupled to a processor, wherein the video  
2 encoder/decoder is configured by the processor a first time to encode/decode data in  
3 accordance with a first one of a plurality of data compression/decompression standards.

1                   2.       The video encoder/decoder of claim 1, wherein the video  
2 encoder/decoder is configured by the processor a second time only if a second one of the  
3 plurality of data compression/decompression standards different from the first one of the  
4 plurality of data compression/decompression standards is selected for encoding/decoding.

1                   3.       The video encoder/decoder of claim 2 wherein the video  
2 encoder/decoder is configured by configuring a configuration register disposed within the  
3 video encoder/decoder.

1                   4.       The video encoder/decoder of claim 3 further comprising a memory  
2 which stores the configuration data for each of the plurality of the data  
3 compression/decompression standards, wherein the processor reads the configuration data  
4 from the memory and loads the same into the configuration register.

1                   5.       The video encoder/decoder of Claim 1 further comprising a vector  
2 pipeline unit, the vector pipeline unit further comprising:  
3                   a run-length decoder which receive data elements of a data vector at its input  
4 terminals and decodes and supplies to its output terminals one of the data elements received  
5 thereby if the run-length decoder is disabled and a run-length of the data elements received  
6 thereby if the run-length decoder is enabled, wherein each data element comprises a plurality  
7 of bits.

1                   6.       The video encoder/decoder of Claim 5 wherein the run-length decoder  
2 is disabled if a bit associated therewith in the configuration register is reset.

1                   7.       The video encoder/decoder of Claim 6 wherein the vector pipeline unit  
2 further comprises:  
3                   an ALU having a plurality of first input terminals which receive the data  
4 element supplied thereto by the run-length decoder, a plurality of second input terminals  
5 which receive a second data element of the vector and a plurality of output terminals; the  
6 ALU to deliver to its output terminals one of a result of a plurality of arithmetic or logic

7 operations performed thereby if the ALU is enabled and the first data element received at its  
8 first input terminals if the ALU is disabled.

1 8. The video encoder/decoder of Claim 7 wherein the ALU is disabled if  
2 a bit associated therewith in the configuration register is reset.

1 9. The video encoder/decoder of Claim 8, wherein the vector pipeline  
2 unit further comprises:

3 a multiplier/divider having a plurality of first input terminals which receive  
4 the data supplied to the output terminals of the ALU, a plurality of second input terminals  
5 which receive a third data element of the vector, the multiplier/divider to supply to its output  
6 terminals a result of one of a plurality of multiplication/division operations performed thereby  
7 if the multiplier/divider is enabled and the data received at its plurality of first input terminals  
8 if the multiplier/divider is disabled.

9 10. The video encoder/decoder of Claim 9 wherein the multiplier/divider is  
10 disabled if a bit associated therewith in the configuration register is reset.

11 11. The video encoder/decoder of Claim 10, wherein the vector pipeline  
12 unit further comprises:

13 a multiplexer having a plurality of first input terminals which receive a fourth  
14 data, a plurality of second input terminals which receive the data supplied to the output  
15 terminals of multiplier/divider, a third input terminal and a plurality of output terminals,  
16 wherein the third input terminal selects and transfers to the multiplexer's output terminals one  
17 of the data supplied to the multiplexer by the multiplier/divider and the fourth data.

1 12. The video encoder/decoder of Claim 11 wherein the multiplexer  
2 transfers to its output terminals the data supplied thereto by the multiplier/divider if a bit  
3 associated with the multiplexer in the configuration register is reset.

1 13. The video encoder/decoder of Claim 12, wherein the vector pipeline  
2 unit further comprises:

3 an accumulator having a plurality of first input terminals which receive the  
4 data supplied to the multiplexer's output terminals, and a plurality of second input terminals  
5 which receive the second data element of the vector, the accumulator to supply to its output

6 terminals a result of one of a plurality of arithmetic operations performed thereby if the  
7 accumulator is enabled and the data received at its plurality of first input terminals if the  
8 accumulator is disabled.

1 14. The video encoder/decoder of Claim 13 wherein the accumulator is  
2 disabled if a bit associated therewith in the configuration register is reset.

1 15. The video encoder/decoder of Claim 14, wherein the vector pipeline  
2 unit further comprises:

3 a barrel shifter having a plurality of first input terminals which receive the  
4 data supplied to the output terminals of the accumulator, wherein the barrel shifter right shifts  
5 the data it receives at its plurality of first input terminals if the barrel shifter is enabled.

1 16. The video encoder/decoder of Claim 15 wherein the barrel shifter  
2 supplies the data it receives at its plurality of first input terminals if the barrel shifter is  
3 disabled.

1 17. The video encoder/decoder of Claim 16 wherein the barrel shifter is  
2 disabled if a bit associated therewith in the configuration register is reset.

1 18. The video encoder/decoder of Claim 8, wherein the vector pipeline  
2 unit further comprises a round logic unit which receives the data supplied thereto by the  
3 barrel shifter and rounds the received data to a nearest integer number, wherein the vector  
4 pipeline unit further comprises:

5 a round logic unit which receives the data supplied thereto by the barrel  
6 shifter and rounds the received data to a nearest integer number if the round logic is enabled,  
7 wherein the round logic unit supplies the rounded data to its output terminals.

1 19. The video encoder/decoder of Claim 18, wherein the round logic unit  
2 delivers to its output terminals the data supplied thereto by the barrel shifter if the round logic  
3 unit is disabled.

1 20. The video encoder/decoder of Claim 19 wherein the round logic unit  
2 is disabled if a bit associated therewith in the configuration register is reset.

1                   21.     The video encoder/decoder of Claim 20, wherein the vector pipeline  
2 unit further comprises:

3                   a modify logic unit which receives the data supplied thereto by the round  
4 logic unit and modifies the received data to one of odd and even number if the modify logic  
5 unit is enabled, wherein the modify logic unit supplies the modified data to its output  
6 terminals.

1                   22.     The video encoder/decoder of Claim 21, wherein the modify logic unit  
2 delivers to its output terminals the data supplied thereto by the round logic unit if the modify  
3 logic unit is disabled.

1                   23.     The video encoder/decoder of Claim 22 wherein the modify logic unit  
2 is enabled or disabled by varying a bit associated therewith in the configuration register.

1                   24.     The video encoder/decoder of Claim 8, wherein the vector pipeline  
2 unit further comprises:

3                   a saturate logic unit which receives the data supplied thereto by the modify  
4 logic unit, the saturate logic unit to saturate the received data to a saturate high value if the  
5 received data is greater than the saturate high value and if the saturate logic unit is enabled,  
6 the saturate logic unit to saturate the received data to a saturate low value if the received data  
7 is smaller than the saturate low value and if the saturate logic unit is enabled, wherein the  
8 saturate logic unit supplies to its output terminals the saturated data.

1                   25.     The video encoder/decoder of Claim 24 wherein the saturate logic unit  
2 supplies to its output terminals data it receives from the output terminals of the modify logic  
3 unit if the saturate logic unit is disabled.

1                   26.     The video encoder/decoder of Claim 25 wherein the saturate logic unit  
2 is enabled or disabled by varying a bit associated therewith in the configuration register.

1                   27.     The video encoder/decoder of Claim 26, wherein the vector pipeline  
2 unit further comprises a status register which collects data supplied thereto by the saturate  
3 logic unit and supplies the collected data to a processor, if the status register is enabled.

1                   28.     The video encoder/decoder of Claim 27 wherein the status register is  
2 enabled or disabled by varying a bit associated therewith in the configuration register.

1           29.     The video encoder/decoder of Claim 8, wherein the vector pipeline  
2 unit further comprises a run-length encoder which receives and encodes the run-length of the  
3 data that is supplied thereto by the saturate logic unit if the run-length encoder is enabled.

1           30.     The video encoder/decoder of Claim 27 wherein the run-length  
2 encoder is enabled or disabled by varying a bit associated therewith in the configuration  
3 register.

1           31.     A method of encoding/decoding video data, the method comprising  
2 the acts of:  
3                 coupling a processor to a video encoder/decoder;  
4                 configuring the encoder/decoder via the processor a first time to  
5 encode/decode data in accordance with a first one of a plurality of data  
6 compression/decompression standards; wherein after the video encoder/decoder is configured  
7 it encodes/decodes data according to the first compression/decompression standard.

8           32.     The method of Claim 31 further comprising the act of:  
9                 configuring the encoder/decoder via the processor a second time only if a  
10                second one of the plurality of data compression/decompression standards different from the  
11                first one of the plurality of data compression/decompression standards is selected; wherein  
12                after the video encoder/decoder is configured the second time it encodes/decodes data  
13                according to the second one of the plurality of data compression/decompression standards.

1           33.     The method of Claim 32 further comprising the act of:  
2                 configuring the encoder/decoder by configuring a configuration register  
3 disposed therein.

1           34.     The method of Claim 33 further comprising the act of:  
2                 storing the configuration data for each of the plurality of compression  
3 standards in a memory.

1           35.     The method of Claim 34 further comprising the acts of:  
2                 reading the configuration data stored in the memory; and  
3                 loading the configuration data read from the memory into the configuration  
4 register.

